REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Office Action of November 15, 2007. Applicants respectfully submit that Kim is not prior art to the present application. Furthermore, Applicants submit that the pending claims are patentable over the cited references for at least the reasons discussed herein.

Kim is Not Prior Art to the Present Application

Claims 12-30 stand rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent No. 7,002,207 to Kim *et al.* (hereinafter "Kim"). *See* Office Action, page 3. Kim was filed on July 1, 2003. The present application claims priority to Korean Patent Application No. 2003-30883, filed on May 15, 2003. Thus, the priority date of the present application is May 15, 2003, which predates the filing date of Kim, July 1, 2003. Applicants provide a certified translation of Korean Patent Application No. 2003-30883, filed on May 15, 2003 herewith. Accordingly, Applicants submit that Kim is not prior art to the present application. Thus, Claims 12-30 are patentable over Kim for at least the reasons discussed herein.

The Section 102 Rejections

Claims 12-19 and 30 stand rejected under 35 U.S.C. § 102 as being anticipated by United States Patent No. 5,583,362 to Maegawa (hereinafter "Maegawa"). *See* Office Action, page 4. Applicants respectfully submit that many of the recitations of these claims are neither disclosed nor suggested by Maegawa. For example, Claim 12 recites:

> A method of forming a unit cell of a metal oxide semiconductor (MOS) transistor, comprising:
>
> forming a MOS transistor on an integrated circuit substrate including an isolation layer and an active region higher than the isolation layer, the MOS transistor having a source region and a drain region on the isolation layer, and a plurality of gates on the active region, the plurality of gates being stacked between the source region and the drain region;
>
> forming a horizontal channel between the source and drain regions, the horizontal channel including at least two horizontal channel regions formed in spaced apart patterns, **wherein the source and drain regions are vertically formed to cover the sides of the active region in other patterns adjacent to sides of the spaced apart patterns; and**

forming a vertical source electrode electrically connected to the source region and a vertical drain electrode electrically connected to the drain region.

Applicants respectfully submit that at least the highlighted recitations of Claim 12 are neither disclosed nor suggested by Maegawa for at least the reasons discussed herein.

The Office Action points to Figure 30 of Maegawa as teaching all the recitations of Claim 12. *See* Office Action, pages 5-6. The Office Action admits that the source and drain are not illustrated in Figure 30, but concludes that a source and drain are inherently required. *See* Office Action, page 5. Applicants agree that MOS transistors inherently have a source and a drain. However, Applicants respectfully submit that Claim 12 recites "...wherein the source and drain regions are vertically formed to cover the sides of the active region in other patterns adjacent to sides of the spaced apart patterns; and forming a vertical source electrode electrically connected to the source region and a vertical drain electrode electrically connected to the drain region." The specific recitation in Claim 12 detailing the source and drain region of Claim 12 is clearly not inherent in Figure 30 of Maegawa. In fact, the final recitation of "forming a vertical source electrode..." of Claim 12 is not even addressed in the Office Action. Accordingly, Applicants respectfully submit that Claim 12 and the claims that depend therefrom are patentable over Maegawa for at least the reasons discussed herein.

Furthermore, Claim 30 recites:

> A method of forming a unit cell of a metal oxide semiconductor (MOS) transistor, comprising:
> **forming a horizontal channel between the source and drain regions, the horizontal channel including at least two horizontal channel regions formed in spaced apart patterns; and**
> **forming source and drain regions in other patterns at sides of the spaced apart patterns**.

Applicants respectfully submit that at least the highlighted recitations of amended Claim 30 are neither disclosed nor suggested by Maegawa for at least the reasons discussed herein.

In particular, the Office Action points to Figure 30 of Maegawa as teaching the channel region as recited in Claim 30 of the present application. *See* Office Action, page 5. The Office Action admits that the source and drain are not illustrated in Figure 30, but concludes that a source and drain are inherently required. *See* Office Action, page 5. Applicants agree that MOS transistors inherently have a source and a drain. However, Applicants respectfully submit that Claim 30 recites "forming a horizontal channel between

the source and drain regions, the horizontal channel including at least two horizontal channel regions formed in spaced apart patterns; and forming source and drain regions in other patterns at sides of the spaced apart patterns." Applicants respectfully submit, that the specific recitations in Claim 30 detailing the source and drain region of Claim 30 are clearly not inherent in Figure 30 of Maegawa. Furthermore, Claim 30 recites that the at least two horizontal channel regions and the source and drain regions are formed in separate patterns, for example, epitaxial layers. Nothing in Maegawa discloses or suggests at least these recitations of amended independent Claim 30. In fact, Maegawa discloses forming the source and drain regions in the same pattern as the horizontal channel. Accordingly, Applicants respectfully submit that Claim 30 is patentable over Maegawa for at least the reasons discussed herein.

The Section 103 Rejections

Claims 20-29 stand rejected under 35 U.S.C. § 103 as being unpatentable over Maegawa in further view of United States Patent No. 6,420,758 to Nakajima (hereinafter "Nakajima"). *See* Office Action, page 8. Applicants respectfully submit that many of the recitations of these claims are neither disclosed nor suggested by the cited references. For example, independent Claim 23 recites, in part:

> A method of fabricating a transistor comprising:
> forming a trench region on an integrated circuit substrate to define an active region;
> forming a stacked structure including at least one set of first epitaxial patterns and second epitaxial patterns on the active region;...
> growing a third epitaxial layer on sidewalls of at least one set of first and second epitaxial patterns;...
> selectively etching the first epitaxial patterns of the set of at least one first and second epitaxial patterns to form a horizontal channel region having a plurality of spaced apart channel layers...

Applicants respectfully submit that at least portions of Claim 23 set out above are neither disclosed nor suggested by the cited combination for at least the reasons discussed herein.

In particular, the Office Action points to Maegawa as teaching the "selectively etching" step of Claim 23. *See* Office Action, page 12. The cited portion of Maegawa discusses a first conductive pattern (channel pattern or gate pattern) having a space and second conductive pattern covering the first conductive pattern after forming a gate insulating

layer. The channel patterns are formed by repeating the formation of the first and second conductive patterns. The process discussed in Maegawa may include a complicated alignment process due to the repeated formation of multiple layers. In stark contrast, Claim 23 recites "selectively etching the first epitaxial patterns of the set of at least one first and second epitaxial patterns to form a horizontal channel region having a plurality of spaced apart channel layers." Nothing in Maegawa discloses or suggests selectively etching the first epitaxial layer to form the channel region as recited in independent Claim 23. Furthermore, nothing in Maegawa discloses or suggests forming a third epitaxial layer on sidewalls of the first and second eptaxial layers as recited in Claim 23. Accordingly, Applicants respectfully submit that independent Claim 23 and the claims that depend therefrom are patentable over the cited combination for at least the reasons discussed herein.

Furthermore, the Office Action cites to embodiment 1 of Maegawa as teaching the step of forming the trench as recited in Claim 23 and embodiment 16 of Maegawa as teaching the step of forming the stacked structure as recited in Claim 23. Maegawa recites "the transistor in Embodiment 15 has a channel silicon film formed of two layer 3a and 3b. However, further multiple layers of channel silicon film, e.g., three, four or more layers may be formed." Thus, Maegawa clearly recites that embodiment 16 is a modification of embodiment 15, not embodiment 1. The Office Action arbitrarily combines the embodiments of Maegawa to teach the recitations of Claim 23 without any motivation besides Applicants' disclosure, which is an inappropriate basis for combination. Accordingly, Applicants respectfully submit that independent Claim 23 and the claims that depend therefrom are patentable over the cited combination for at least these additional reasons discussed herein.

CONCLUSION

Applicants respectfully submit that pending claims are in condition for allowance, which is respectfully requested in due course. Favorable reconsideration of this application is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,

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CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on March 14, 2008.

Candi L. Riggs